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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **DONALD E. DEMMING, ET AL.**	§	Docket No. **TU9-98-010**
Serial No. **09/131,846**	§	Examiner: **BRYCE P. BONZO**
Filed: **July 24, 1998**	§	Art Unit: **2114**
For: **DATA PROCESSING METHOD AND SYSTEM FOR SIMULATION OF HARDWARE FAULTS UTILIZING A PCI BUS**	§	

APPEAL BRIEF UNDER 37 C.F.R. §1.192

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Sir:

This Brief is submitted in support of the Appeal in the above-identified application.

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(A)]

I hereby certify that this correspondence is being:

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August 5, 2005 — Date

Jane Graham — Jane Graham

REAL PARTY IN INTEREST

The real party in interest in the present Appeal is International Business Machines Corporation (*IBM*), the Assignee of the present Application as evidenced by the Assignment set forth at Reel 9383, Frame 0621.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, the Appellant's legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-18 stand finally rejected as noted in the Examiner's Action dated March 8, 2005.

STATUS OF AMENDMENT

No Amendment has been submitted subsequent to the Final Rejection in the present Application.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Claims 1 and 10 set forth a method and system for simulating a hardware fault occurring on an expansion card coupled to a data processing system utilizing a bus. A fault simulator card 18 is illustrated in Figure 2 and described in the present Specification at page 7, line 9, *et seq.* As depicted, fault simulator 18 includes a Digital-to-Analog Converter 30 (DAC), a buffer amplifier 32, a control register 34, multiple relays 36 and multiple relays 37.

DAC 30 and control register 34 both receive as their inputs a control signal 41 which is output by decoder 39. Decoder 39 receives, utilizing PCI box 24, and decodes a signal 38 from processing unit 12. Control signal 41 includes information regarding which line or lines of PCI

bus are to be utilized to test the response of processing unit 12 to a particular hardware fault. Control signal 41 also includes information regarding the test voltage level to be utilized during the simulation.

DAC 30 is then utilized to convert the digital information regarding the test voltage level to the proper analog voltage level. DAC 30 outputs an analog signal 40 having a first voltage level to buffer amplifier 32 which amplifies signal 40 and outputs it as test voltage signal 42. Any number of different test voltage levels can therefore be selected and generated utilizing DAC 30 and buffer amplifier 32. Test voltage signal 42 is then received by multiple relays 36.

Control register 34 also receives information regarding which line or lines of PCI bus 24 are to be utilized to test the response of processing unit 12 to a particular hardware fault. Control register 34 is utilized to turn selected relays 36 and 37 either on or off. Control register 34 is coupled to relay 36a via signal 48, relay 36b via signal 46, relay 36c via signal 44, relay 37a via signal 50, relay 37b via signal 52, and relay 37c via signal 54. Control register 34 includes a bit associated with each signal output from control register 34 which may be either set or reset to drive the signal either HIGH or LOW.

As an example, when a particular hardware fault calls for PCI line 56 to be driven HIGH, control signal 41 includes information which sets a bit in control register 34 associated with signal 48 to drive signal 48 HIGH, and resets a bit in control register 34 associated with signal 50 to drive signal 50 LOW. Relay 36a is turned on while relay 37a is turned off. This causes the test voltage signal 42 to be output on PCI line 56, thus simulating the selected hardware fault at a particular voltage level.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The ground of rejection to be reviewed on appeal is whether or not the Examiner's rejection of Claims 1-18 under 35 U.S.C. §102(e) as anticipated by *Gates*, United Patent Number 5,701,409 is well founded.

ARGUMENT

Gates discloses an integrated circuit which includes a bus error generation circuit coupled to a bus interface terminal of the integrated circuit. After a particular error command is loaded into the command register of the bus error generation circuit of *Gates*, an incorrect parity value is output onto the PCI bus terminal during a subsequent data write PCI bus cycle by XOR gate 109 as depicted in Fig. 3. A target device on the PCI bus then receives that data and the incorrect parity, logs the error condition by setting a bit in its status configuration register, and asserts the parity error signal on PERR# line back to the initiator device. Upon receiving the parity error signal on the PERR# line, the master device sets an appropriate bit in its status configuration register. The command register of the bus error generation circuit is cleared so that the error condition will be generated only once. In this manner *Gates* teaches that the device on the PCI bus which loaded the master device with the error command can read the status configuration registers of the master and target devices over the PCI bus to make sure that the incorrect parity value on the PCI bus was properly detected and handled on the PCI bus.

In the previous appeal in this application the Board of Patent Appeals and Interferences in their decision dated June 30, 2004 noted, while sustaining the Examiner's rejection "it seems to us that appellants' invention may be the use of a DAC to generate the voltage signal representative of a hardware fault, as opposed to the use of logic gates (such as XOR gate 109 in Fig. 3) in *Gates*. However, the examiner correctly noted that a DAC is not claimed. If it was, the examiner would have then tried to find prior art to show the obviousness of using a DAC in place of a logic gate." See the decision of the Board of Patent Appeals and Interferences dated June 30, 2004, pages 5 and 6.

Based upon a careful consideration of the decision of the Board, Applicant filed a continuation and amended the claims in the present application to expressly recite "creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog voltage converter...."

In reiterating his rejection of Claims 1-18 over the *Gates* reference, the Examiner dismisses this amendment and, apparently, the direction of the Board of Patent Appeals and Interferences, and simply notes "the digital-to-analog converter as described by Applicant is inherent to the PCI specification, and is described under the heading response to amendments..." and thereafter notes a belief that the *Gates* reference "clearly provides for this DAC functionality, taking a digital signal and conditioning it through analog manipulation for transport on the PCI bus with vary (*SIC*) different physical requirements than that of the board from which the original digital signal was received."

In response to this boldfaced assertion by the Examiner, Applicant has carefully examined the PCI specification and fails to find a single reference therein to the utilization of a digital-to-analog converter and strenuously disputes the Examiner's characterization of this circuit element as "inherent" within the PCI specification. In support of this position Applicant urges the Board to consider that if the utilization of a digital-to-analog converter is inherent then why does *Gates* teach the utilization of an XOR gate having a digital output, as depicted at element 109 of Fig. 3 of *Gates*?

In summary, the Examiner has taken the position that the Gates reference anticipates the claimed invention set forth in the present application despite the absolute absence of even the slightest scintilla of suggestion for the utilization of a digital-to-analog converter to create an analog voltage signal representative of a specified hardware fault, as expressly set forth within the claims of the present application, and Applicant urges the Board to reverse this rejection as it clearly stretches "inherency" past any reasonable interpretation of the prior art.

Please charge IBM Corporation Deposit Account No. **09-0449** in the amount of $500.00 for submission of a Brief in support of an Appeal. No additional fees or expenses are believed to be required; however, if any additional fees are required, please charge IBM Corporation Deposit Account No. **09-0449**.

Respectfully submitted,

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ATTORNEY FOR APPLICANT

APPENDIX

1. A method in a data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, said method comprising the steps of:

specifying said hardware fault to simulate;

determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;

creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog voltage converter; and

outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated.

2. The method according to claim 1, wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

3. The method according to claim 1, further comprising the step of prior to outputting said analog voltage signal, determining a proper response of said system to said hardware fault.

4. The method according to claim 3, further comprising the step of in response to outputting said analog voltage signal, determining if said system responded properly to said hardware fault.

5. The method according to claim 4, further comprising the step of determining a line of said bus which is associated with said hardware fault.

6. The method according to claim 5, further comprising the step of outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus.

7. The method according to claim 6, further comprising the step of determining a test voltage level for said analog voltage signal, wherein said test voltage level is a voltage level required to simulate said hardware fault.

8. The method according to claim 7, further comprising the step of outputting said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus.

9. The method according to claim 8, wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

10. A data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, comprising:

means for specifying said hardware fault to simulate;

means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;

a digital-to-analog voltage converter for creating an analog voltage signal representative of said specified hardware fault; and

means for outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated.

11. The method according to claim 10, wherein said means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises means for determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.

12. The system according to claim 10, further comprising means prior to outputting said analog voltage signal, for determining a proper response of said system to said hardware fault.

13. The system according to claim 12, further comprising means responsive to outputting said analog voltage signal, for determining if said system responded properly to said hardware fault.

14. The system according to claim 13, further comprising means for determining a line of said bus which is associated with said hardware fault.

15. The system according to claim 14, further comprising means for outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus.

16. The system according to claim 15, further comprising means for determining a test voltage level for said analog voltage signal, wherein said test voltage level is a voltage level required to simulate said hardware fault.

17. The system according to claim 16, further comprising means for outputting said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus.

18. The system according to claim 17, wherein said means for determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises means for determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card.